1. **What general categories of functions are specified by computer instructions?**

*Processor-memory*: Data may be transferred from processor to memory or from memory to processor.

*Processor-I/O*: Data may be transferred to or from a peripheral device by transferring between the processor and an I/O module.

*Data processing*: The processor may perform some arithmetic or logic operation on data.

*Control*: An instruction may specify that the sequence of execution be altered.

1. **List and briefly define the possible states that define an instruction execution**.

* **Instruction address calculation** (iac): Determine the address of the next instruction to be executed.
* **Instruction fetch** (if):  Read instruction from its memory location into the processor.
* **Instruction operation decoding**: Analyze instruction to determine type of operation to be performed and operand(s) to be used
* **Operand address calculation** (oac) : If the operation involves reference to an operand in memory or available via I/O, then determine the address of the operand.
* **Operand fetch** (of): Fetch the operand from memory or read it in from I/O.
* **Data operation**: Perform the operation indicated in the instruction
* **Operand store** (os): Write the result into memory or out to I/O.

1. **List and briefly define two approaches to dealing with multiple interrupts**.

+ Disable all interrupts while an interrupt is being processed.

+ Define priorities for interrupts and to allow an interrupt of higher priority to cause a lower-priority interrupt handler to be interrupted.

1. **What types of transfers must a computer's interconnection structure (e.g. bus) support?**

+ Memory to processor + Processor to Memory.

+ I/O to processor. + Processor to I/O

+ I/O to and from memory

**5. What is the benefit of using a multiple-bus architecture compared to a single-bus architecture?**

- Several buses allow multiple devices to function at the same time, minimizing waiting time and increasing computer speed. The major rationale for having many buses in a computer design is to boost performance.

**01. A MEMORY ADDRESS (MAR) register specifies the address in memory for the next read or write.**

**02. A MOMORY BUFFER (MBR) register contains the data to be written into memory or receives the data read from memory.**

**03. The most common classes of interrupts are: program, timer, I/O and HARDWARE FAILURE**

**04. A(n) TIMER interrupt is generated by a timer within the processor and allows the operating system to perform certain functions on a regular basis.**

**05. A(n) I/O interrupt is generated by an I/O controller to signal normal completion of an operation, request service from the processor, or to signal a variety of error conditions.**

**06. A DISABLED interrupt simply means that the processor can and will ignore that interrupt request signal.**

**07. The collection of paths connecting the various modules is called the INTERCONNECTION** **structure**.

**08. A BUS is a communication pathway connecting two or more devices.**

**09. The CONTROL lines are used to control the access to and the use of the data and address lines.**

**10. Bus lines can be separated into two generic types: DEDICATED and multiplexed.**

**11. With asynchronous timing the occurrence of one event on a bus follows and depends on the occurrence of a previous event.**